Ph.D. Project :
Hardware Autogeneration
for Error-Correction Solutions

General Information

Research area:	Digital circuit design, hardware autogeneration, error-correction coding, and compiler design
Supervisor:	Prof. Pascal Giard <pascal.giard@etsmtl.ca>
Institution:	École de technologie supérieure, Montréal, Québec, Canada
Start date:	Winter 2027 or as early as possible

Context

Error-correction coding is essential to modern communication and storage systems, and its hardware implementation, particularly the decoder, often constitutes the most resource-intensive component of receivers. While high-level synthesis (HLS) tools can automatically generate hardware from high-level descriptions, they often produce designs that are less optimized than hand-crafted ones. Domain-specific hardware autogeneration has proven to be a more effective approach for generating efficient, highly optimized circuits.

Existing works on circuit generation for error correction remain narrow in scope, each supporting only a single code family (e.g., polar codes or LDPC codes) and none featuring a design-space exploration (DSE) optimizer. Developing an open, domain-specific hardware-generation framework that spans multiple families of error-correcting codes and integrates with DSE is an open and impactful research challenge.

This project is part of an NSERC Discovery research program whose long-term objective is to create an open ecosystem for the design-space exploration of error-correction solutions, enabling the informed selection of a code along with the decoding algorithm and hardware architecture, all the way down to the autogeneration of the associated circuits. Furthermore, this program involves collaborations with Prof. François Leduc-Primeau (Polytechnique Montréal), Prof. Camille Leroux (Bordeaux INP, France), and Prof. Stefan Weithoffer (IMT Atlantique, France). Depending on the research direction and the student's interests, opportunities for co-supervision, close collaboration, or international research stays may be available.

Project Objectives

The primary objective of this project is to investigate, design, and develop domain-specific hardware autogeneration capabilities for error-correction decoders, integrated within a DSE framework. More specifically, the project aims to:
- Expand domain-specific intermediate representations (IRs) to capture hardware-specific details, including task mapping, dependencies, dataflow, and architecture descriptions, enabling precise hardware synthesis.
- Explore methods for embedding annotations within the IRs to specify hardware constraints and scheduling parameters that guide hardware generation.
- Develop algorithms for translating the IRs into complete domain-specific hardware architectures, encompassing processing units, interconnects, and control logic.
- Investigate methods for mapping tasks to specific hardware components and generating interconnects based on data dependencies, including techniques for parallel data paths and concurrent execution.
- Research automatic control-unit generation, resource-sharing strategies, and optimization techniques such as loop unrolling and pipelining to improve area, throughput, and energy efficiency.
- Develop automated testbench generation to validate hardware accuracy through simulation.

Expected Contributions

In addition to the doctoral thesis, the project is expected to result in multiple significant contributions disseminated in peer-reviewed publications. Furthermore, here are examples of potential technical contributions tied to this project:
- Hardware-oriented IRs that capture architecture-level details for multiple error-correcting code families.
- A domain-specific compiler capable of translating IRs into synthesizable hardware descriptions, e.g., VHDL.
- Optimization techniques integrated into the generation process, e.g., resource sharing or pipelining.
- Automated testbench generation for simulation-based validation of the generated hardware.

Desired Profile

- Student in electrical engineering, computer engineering, or a closely related field.
- Solid background in digital circuit design, preferably for FPGAs or ASICs.
- Strong skills in hardware description languages (VHDL and/or Verilog).
- Strong programming skills.
- Interest in error-correction coding and decoding algorithms.

The following skills are considered assets:
- Experience with hardware autogeneration or code generation for digital circuits.
- Familiarity with error-correcting codes, e.g., LDPC, Polar, or Turbo codes.
- Experience with compiler design or intermediate representations.
- Knowledge of hardware optimization techniques, e.g., pipelining, resource sharing, or loop unrolling.

Supervision

Supervision will be provided by Professor Pascal Giard. Dr. Giard is a professor in the Department of Electrical Engineering at ÉTS. His research focuses on the efficient implementation of digital systems, from algorithm design to software and hardware realization. He has extensive experience in error-correction coding, hardware architecture design, and the development of design-space exploration tools.

The selected candidate will join a team of graduate student researchers working on closely related topics.

Pascal Giard

Funding and Duration

The project is funded for a duration of four years and includes financial support for the student's stipend as well as research-related expenses, including international conference travel.

Location

ÉTS is located in Montréal, Québec, Canada. Often described as an appealing blend of North American and European culture, Montréal is a safe, multicultural city with a high quality of life and a relatively affordable cost of living. It is the most bilingual and trilingual city in North America: over 50% of Montréalers are fluent in both English and French, and more than 20% speak three or more languages.

Since 2016, Montréal has consistently been ranked the best student city in North America by Quacquarelli Symonds. The city is also well known for its quality of life, proximity to both peaceful rural landscapes and exciting ski resorts, and its vibrant neighborhoods and green spaces. Located in the heart of the city, the ÉTS campus is easily accessible by bicycle or public transportation. Approximately 1,100 students live in the university residences, which include furnished studios and apartments with heating, electricity, and unlimited Internet access.

Since its founding, ÉTS has pursued a mission deeply rooted in all of its activities: addressing the needs of industry, which requires engineers with not only strong theoretical foundations but also practical expertise. To fulfill this mission, ÉTS maintains a unique partnership with the business and industrial sectors, from small enterprises to large corporations. It distinguishes itself from other Québec universities through its applied education model and its research activities conducted by and for industry.

Interested?

Interested candidates should submit their CV, academic transcripts, contact information for appropriate references, and a brief statement of interest (maximum one page) describing how their background is relevant to this project.

Contact: Prof. Pascal Giard <pascal.giard@etsmtl.ca>
Start date: Winter 2027 or as early as possible