Ph.D. Project:
Energy-proportional Polar Decoders

General Informations

Research fields: Error correction and digital circuits
Advisor: Prof. Pascal Giard <pascal.giard@etsmtl.ca>
Starting date: Immediately or to be discussed

Project Context

Forward-error-correction (channel) coding is an essential ingredient of all modern communication systems. Decoders of such codes are often one of the most computationally intensive and power hungry task in modern wireless receivers. One of the latest innovations in channel coding are polar codes, a type of codes that can provably achieve the capacity of all practically relevant channels [1]. The widely-recognized disruptive impact of these codes is illustrated by the recent, rapid adoption of this class of codes as part of 3GPP's next-generation mobile-communication standard (5G) [2]. Besides the communication-performance benefits of polar codes, an important ingredient to their success has been the recent progress in the design of advanced decoding algorithms and corresponding decoders with manageable complexity and power consumption. Nevertheless, compared to the achievements of 20+ research years in efficient decoder design for the competing low-density parity-check (LDPC) and turbo codes, polar decoders are still in their infancy, lagging behind in terms of area and energy efficiency [3]. An important and fundamental reason for the limited (area and energy) efficiency of today's polar decoders is deeply rooted in the nature of close-to-optimal decoding strategies. These advanced algorithms explore multiple hypotheses to maximize the chance for success, i.e., finding the correct codeword. Unfortunately, in order to always meet expectations on sampling rate, throughput, and latency, all of these hypotheses must typically be considered in parallel whereas the competing codes use iterative schemes. In practice, this leads to severe overhead, notably in terms of area and power consumption, which is unnecessary under the most frequent operating conditions. Most of the resources are wasted on calculations that are, in the end, discarded.

The proposed research focuses on the creation of novel algorithms and decoder implementations (software or hardware) for polar codes that are energy efficient while catering sufficient quality for the application. The main motivation is to advance the state of the art in energy-efficient decoding of polar codes to enable their application in emerging and future wireless communication systems. However, despite this specific objective and application, our approach is motivated by the rather generic observation that the implementation of many signal-processing systems (especially in communications) is often driven by real-time constraints commonly translated into hard deadlines and throughput requirements for their various components. These stringent design requirements are an obstacle to the use of algorithms that exhibit a strongly variable complexity. In fact, algorithms with a fixed complexity are regularly preferred, at the expense of a potentially significant area and average-energy overhead, over algorithms that are on average more economic, but have a variable and sometimes even unbounded maximum complexity.

Project Description

Energy-proportional decoding algorithms, by nature, have a variable execution time. This property has complicated the integration of their implementations into traditional receiver architectures which typically enforce a constant throughput, a constraint that can be matched in a straightforward fashion by designing for the worst case. This however results in a highly inefficient and over-designed hardware implementation. Hence, this type of decoder has received little attention in terms of implementation as a standalone component and its integration into an overall system has not been addressed at all.

Being fundamentally the most energy-efficient decoding algorithm, we are deeply convinced that Successive-Cancellation Flip (SCFlip) decoding of polar codes [4], [5] bears great potential for 5G applications. Yet, because it received little scrutiny, the primary objective of the student will be to improve this algorithm further to reduce the gap between the worst-case execution time and the average case. Thus, this student will start by performing an in-depth review of the recent advances on this algorithm as well as in the other polar decoding algorithms with the aim of adapting some of these techniques to improve SCFlip. He will also devise an early-termination scheme

for undecodable frames. This student will then propose algorithmic improvements to SCFlip and validate them by implementing the new decoding algorithm in software, integrating it into a simulation framework.

Lastly, the student will design a hardware architecture of the improved SCFlip algorithm. Then, he will implement his architecture on FPGA to conduct energy-efficiency experimentations and optimizations.

Supervision and Funding

Supervision will be provided by Prof. Pascal Giard, a newly appointed professor in the electrical engineering department of the École de technologie supérieure (ÉTS). Professor Giard's research is on the efficient implementation of digital systems, from algorithm design to software and/or hardware implementation. His research led to 3 patents, 1 reference book, 10 journal articles, and 19 conference articles. According to Google Scholar, his work has been cited over 550 times over the course of the last 5 years.

Funding is secured for the complete duration of the Ph.D. (amounts to be discussed).

Profile Requirements

- Master in electrical engineering or equivalent
- Research experience in a field related to the topic is an asset
- Proefficiency in prototyping of algorithms
- Proefficiency in implementing algorithms in software (either desktop CPUs or embedded systems or GPUs)
- Proefficiency in implementing algorithms in hardware (VHDL preferred)
- Interest in the field of decoders for modern error-correcting codes
- Some knowledge of SIMD instructions (x86-64 or ARM) is a plus
- Experience with FPGA implementation is a plus
- Some knowledge about modern error-correcting codes is a plus
- Some knowledge about GNU Radio, a software-defined-radio framework, is a plus

How to Apply

Send an email to the supervisor with the subject title as the subject line, including a full CV, university transcripts, recommendation letters and/or contacts from the former lecturers/teachers/advisors, and a short statement (max. 1 page) describing how your experience is beneficial for you to successfully carry out this project.

References

[1] E. Arıkan, "Channel polarization: A method for constructing capacity-achieving codes," in *IEEE Int. Symp. on Inf. Theory (ISIT)*, Jul. 2008, pp. 1173–1177. DOI: 10.1109/TIT.2009.2021379. arXiv: 0807.3917.

[2] MCC Support, *Final Report of 3GPP TSG RAN WG1 #87 v1.0.0*, Feb. 2017.

[3] A. Balatsoukas-Stimming, P. Giard, and A. Burg, "A comparison of polar decoders with existing LDPC and turbo decoders," in *IEEE Wireless Commun. and Netw. Conf. (WCNC)*, San Francisco, CA, USA, Mar. 2017, pp. 1–6. DOI: 10.1109/WCNCW.2017.7919106. arXiv: 1702.04707.

[4] O. Afisiadis, A. Balatsoukas-Stimming, and A. Burg, "A low-complexity improved successive cancellation decoder for polar codes," in *Asilomar Conf. on Signals, Syst., and Comput. (ACSSC)*, 2014, pp. 2116–2120. DOI: 10.1109/ACSSC.2014.7094848. arXiv: 1412.5501.

[5] P. Giard and A. Burg, "Fast-SSC-Flip decoding of polar codes," in *IEEE Wireless Commun. and Netw. Conf. (WCNC)*, Barcelone, ESP, Apr. 2018, pp. 73–77. DOI: 10.1109/WCNCW.2018.8369026. arXiv: 1712.00256.